FLOATING POINT UNIT FOR MULTIPLE DATA ARCHITECTURES

ABSTRACT OF THE INVENTION

An embodiment of the present invention provides a computer system with a floating point unit ("FPU") for supporting multiple floating point architectures. Multiple floating point architectures are supported by an FPU with an internal data-flow format that accommodates formats of each architecture. The system includes a format converter for converting between the internal data flow format and the architected external data types by multiplexing the exponent. The system includes a floating point unit having an internal data-flow according to an internal floating point format for performing floating point operations. The internal format has a number of exponent bits sufficient to support each of the plurality of floating point architectures and the internal format has a number of fraction bits sufficient to support each of the plurality of floating point architectures. The system also includes format converters for converting the exponent value of each floating point architecture into the internal floating point format so that a data operand of any of the floating point architectures input to the floating point unit is converted into the internal floating point format for subsequent arithmetic operations, and the result of the operation is converted back into the original floating point architecture by converting the exponent value of the result from the internal floating point format into the original floating point architecture.